REMARKS

Applicant thanks the Examiner for the careful review of this application. Claims 36-49 remain pending in this application.

Rejection under 35 U.S.C. § 103(a)

Claims 36-39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,272,153 to Huang et al. (hereinafter "Huang").

Claims 40-44 and 47 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang in view of U.S. Patent No. 6,449,519 to Kuwaoka (hereinafter "Kuwaoka").

Claims 45-46 and 48-49 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang as modified by Kuwaoka in further view of U.S. Patent No. 6,233,562 to Sueyoshi et al. (hereinafter "Sueyoshi").

Applicant respectfully traverses for the following reasons.

Prior Art

Huang teaches an audio decoder architecture that uses various component sharing techniques to conserve hardware and reduce implementation costs. [Huang, col. 2, lines 27-30]. Huang teaches an audio decoder comprises a host interface, an input buffer, a bitstream, a synchronization controller, an MPEG audio decode controller, an AC3 audio decode controller, a bypass controller, an output interface, a set of controller multiplexers, an address generator, a memory module, a data path module, and an output buffer. [Huang, col. 7, lines 32-42] The host interface 502 is coupled to the sync controller 508. [Huang, col. 7 line 45, Fig.5] Figure 5 has been reproduced for convenience below:

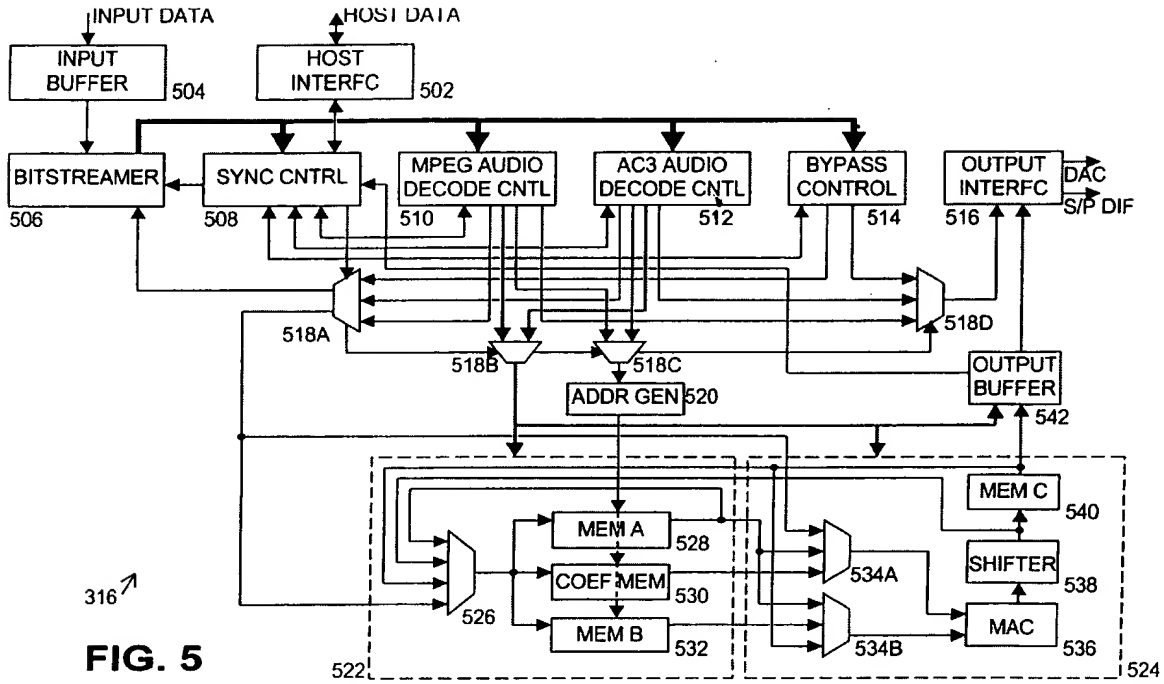

FIG. 5

The host interface 502 communicates read and write status and configuration information to registers in the sync controller 508. [Huang, col. 7, lines 46-48, Fig. 5] Moreover, the input buffer 504 is coupled to the bitstreamer 506 which is coupled to the sync controller 508. [Huang, Fig. 5] At the beginning of each audio data frame, the sync controller 508 is in control of the bitstreamer 506. [Huang, col. 8, lines 8-10, Fig. 5] The sync controller 508 parses the audio data frame headers and extracts audio data format information. [Huang, col. 7, line 66 – col. 8 line 1, Fig. 5] Once the sync controller 508 extracts the audio data format information, a set of multiplexers 518, controlled by the sync controller 508, routes the data to one of three decode/controllers 510, 512, 514 to decode the audio signal. [Huang, col. 8, lines 19-28, Fig. 5] The three decode/controllers include an MPEG audio decode controller 510, an AC3 decode controller 512, and a bypass control 514. [Huang, Fig. 5] The MPEG audio decode controller 510 and the AC3 audio decode controller 512 decode the audio data compressed according to the corresponding standard while the bypass

control 514 operates to bypass the decoding process and forwards the information to the output buffer. [Huang, col.8, lines 13-19, Fig. 5]

In the office action, the examiner has equated the host interface 502 with a write address generator, the sync controller 508 with a memory controller, and the MPEG audio decode controller 510 and the AC3 decode controller 512 with an audio format detection. [Huang, Fig. 5] Huang teaches that the host interface 502 can be coupled to the sync controller 508, not the MPEG audio decode controller 510 or the AC3 decode controller 512, as illustrated by the excerpt below:

> "The host interface 502 couples to controller 302 to allow controller 302 to read and write status and configuration information to registers in sync controller 508." [Huang, col. 7, lines 45-48, Fig. 5]

Thus, Huang does not teach a write address generator coupled to the audio format detection and the memory controller.

Further, the applicant respectfully submits that the MPEG audio decode controller 510 and the AC3 audio decode controller 512 are not used for audio format detection. Huang teaches that the sync controller extracts audio data format information and determines which of the controllers 510, 512, or 514 will control the processing of the audio data, as illustrated by the excerpt below:

> "Sync controller 508 implements a state machine for parsing the audio data frame headers and extracting bitstream side information (BSI) such as audio data format, bit rate, and sampling frequency." [Huang, col. 7, line 66 – col. 8 line1]

The MPEG audio decoder 510 and the AC3 audio decoder 512 then carry out the decoding of audio data according the corresponding standard. [Huang, col. 8, lines 13-16, Fig. 5] Therefore, Huang does not teach audio format detection by the MPEG audio decoder 510 and the AC3 audio decoder 512.

Prior Art Distinguished

In contrast to Huang, Claim 36 contains the language, "a write address generator coupled to the audio format detection and memory controller." As discussed above, the examiner has equated the host interface 502 with a write address generator, the sync controller 508 with a memory controller, and the MPEG audio decode controller 510 and the AC3 decode controller 512 with an audio format detection. Huang teaches that the host interface 502 is coupled only to the sync controller 508. Huang does not teach that the host interface 502 is coupled to the MPEG audio decode controller 510 or the AC3 decode controller 512, as illustrated by the excerpt below:

> "The host interface 502 couples to controller 302 to allow controller 302 to read and write status and configuration information to registers in sync controller 508." [Huang, col. 7, lines 45-48, Fig. 5]

Thus, Huang does not teach "a write address generator coupled to the audio format detection and memory controller." Therefore, Huang does not render Claim 36 unpatentable. For at least these reasons, the independent Claim 36 is allowable over the teachings of Huang.

Further, in contrast to Huang, Claim 36 contains the language "an audio format detection coupled to the first FIFO register and operative to detect a format of the

digital audio signal." As discussed above, the examiner has equated the MPEG audio decode controller 510 and the AC3 audio decode controller 512 with the audio format detection. Huang teaches the sync controller 508 extracts audio data format information and determines which of the controllers 510, 512, or 514 will control the processing of the audio data, as illustrated by the excerpt below:

> "Sync controller 508 implements a state machine for parsing the audio data frame headers and extracting bitstream side information (BSI) such as audio data format, bit rate, and sampling frequency." [Huang, col. 7, line 66 – col. 8 line1]

Thus, Huang does not teach that the MPEG audio decode controller 510 and the AC3 audio decode controller 512 "detect a format of the digital audio signal." Therefore, Huang does not render Claim 36 unpatentable. For at least these additional reasons, the independent Claim 36 is allowable over the teachings of Huang.

Claims 37-49 are either directly or indirectly dependent on the independent Claim 1. As described above, the independent Claim 1 is allowable over the teachings of Huang. Accordingly, Claims 37-49 are also at least allowable as being dependent on an allowable claim.

Applicant respectfully submits that discussion of Kuwaoka and Sueyoshi is unnecessary in light of the above arguments as the claims are patentable over the teachings of Huang and are in condition for allowance.

CONCLUSION

Applicant believes that all pending claims are now allowable. The applicant respectfully requests that all objections and rejections be withdrawn and a Notice of Allowance be issued at the earliest possible date.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel at the number set out below.

Respectfully submitted,
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